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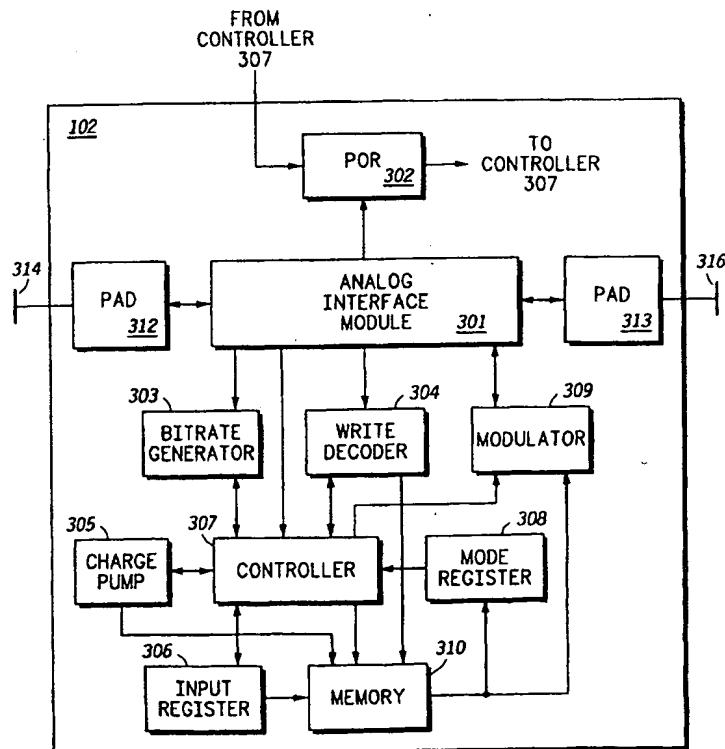
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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## (54) Title: ELECTROSTATIC RFID/EAS SYSTEM

## (57) Abstract

An electrostatic radio frequency identification (RFID)/electronic article surveillance (EAS) system (100) is presented. Under the present invention, the electrostatic RFID/EAS system can perform an RFID data transfer function as well as an EAS function. During an RFID operating mode (308) data transfer from the memory (310) of the transponder (102) is delayed by a predetermined period. After such delay, if the exciter signal is still received, data transfer is carried out. During an EAS operating mode, an alarm signal is generated and transmitted in place of the data information. In an alternative embodiment, a dedicated electrostatic EAS system is presented.



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## ELECTROSTATIC RFID/EAS SYSTEM

Field of the Invention

5 The invention generally relates to radio frequency identification (RFID) technology, and more particularly relates to contactless programmable electrostatic RFID technology.

Background of the Invention

10 Radio frequency identification (RFID) technology allows identification data to be transferred remotely which provides a significant advantage in identifying persons, articles, parcels, and others. In general, to access identification data stored in a RFID transponder (also referred to as a tag or a transceiver) remotely, a RFID reader generates an energy field to activate the RFID transponder and subsequently to retrieve data stored in the transponder unit from a distance. The data retrieved is then processed by a host computer system to identify the person or article that is associated with the transponder. RFID technology has found a wide range of applications including tracking, access control, theft prevention, 20 security, etc.

For some applications, RFID technology is more preferable than magnetic stripe technology, which also finds applications in a few of the areas above. The reason is systems employing RFID technology can store more information than magnetic stripe technology. Moreover, magnetic 25 stripe technology requires relatively high maintenance (e.g., head cleaning). Furthermore, magnetic stripe technology is prone to card and reader damage, corruption or loss of data due to unintentional magnetic field exposure, etc.

RFID technology should be distinguished from radio identification 30 (radio ID) technology that uses radio waves, or more precisely far field electromagnetic (EM) waves which is also known as radiation waves. Far field means the distance between the transponder and reader is great compared to the wavelength of the EM carrier signal used. An example of radio ID technology is the identify friend or foe (IFF) systems used with

military aircraft. Far field EM waves have a field strength that varies inversely with the distance involved.

In contrast, conventional RFID technology is based upon inductive coupling utilizing magnetic field waves. Conventional RFID technology 5 operates in the near field where the operating distance is far less than one wavelength of the EM field. Unlike far field radio waves, the magnetic field strength is approximately proportional to the inverse cube of the distance from the source. In inductance-based RFID technology, an electromagnetic field is generated for use both as a power source for the 10 transponder and for transferring data and clock information between the reader and transponder. Magnetic fields are generated by causing an alternating current to flow in coils that typically have multiple turns. However, it is difficult to integrate these coils in an integrated circuit. Generally, these coils are required to be wire wound or etched metal. This 15 requirement adversely impacts the costs, manufacturability, and packaging flexibility of inductance-based RFID technology. Due to the prohibitive costs and high degree of manufacturing difficulty, electromagnetic RFID technology is not practical in high volume/low cost disposable applications. The bulky packaging, which is typical for electromagnetic RFID technology, 20 further limits its application to those where thickness is not of primary importance.

In general, an electronic article surveillance (EAS) system is designed to prevent article thefts and is widely used in retail stores as well as libraries. An EAS system is typically implemented such that an EAS 25 transponder (tag) is inserted into or attached to an article. Operationally, an EAS reader/detector transmits an activation signal. When the EAS transponder receives the activation signal, it becomes activated and sends back a response signal. Accordingly, unless the EAS transponder has been removed from the article or deactivated by the attendant, it triggers 30 the reader/detector to sound an alarm that alerts the attendant of a potential theft. The activation signal generated by an EAS reader/detector has been known to falsely activate a RFID transponder to transmit its stored information that is undesirable.

For versatility, it is desirable to have a RFID system that can also function as an EAS system. Given the high costs, difficult manufacturability, and packaging inflexibility of conventional RFID technology, it is impractical to combine these two functions into a single 5 transponder in high volume/ low cost disposable applications. It is also desirable to have an alternate EAS system that is inexpensive, easy to manufacture, and allows for packaging flexibility.

Thus, a need exists for an apparatus and system to combine a RFID function with an EAS function in the same system that is inexpensive, easy 10 to manufacture, and allows for packaging flexibility. A need also exists for an apparatus and system for article theft prevention that is less expensive than RFID, easy to manufacture, and allows for packaging flexibility.

#### Brief Description of the Drawings

15 FIG. 1 is a high-level block diagram illustrating an exemplary electrostatic radio frequency identification (RFID) system that implements the present invention.

FIG. 2 is a block diagram illustrating in greater detail electrostatic RFID reader illustrated in FIG. 1.

20 FIG. 3 is a block diagram illustrating in greater detail an electrostatic RFID transponder (tag) illustrated in FIG. 1.

FIG. 4 is a block diagram illustrating in greater detail an analog interface module illustrated in FIG. 3.

25 FIG. 5 illustrates an exemplary mapping of the contents of a memory.

FIG. 6 illustrates the lock bit and the individual configuration bits from the configuration block (block 0) of the memory.

FIG. 7 is a block diagram illustrating in greater detail a power on reset (POR) circuit illustrated in FIG. 3.

30 FIG. 8 is a timing diagram illustrating, as an example, a continuous exciter signal generated by electrostatic RFID reader in accordance to the present invention.

FIG. 8A illustrates a timing diagram of the transponder in response to the continuous exciter signal in FIG. 8 without the time delay of the present invention.

FIG. 8B illustrates a timing diagram of the transponder in response 5 to the continuous exciter signal in FIG. 8 with the time delay of the present invention.

FIG. 9 is a timing diagram illustrating, as an example, a pulsed exciter signal generated by an electrostatic electronic article surveillance (EAS) reader.

10 FIG. 9A illustrates a timing diagram of transponder in response to the pulsed exciter signal in FIG. 9 without the time delay of the present invention.

FIG. 9B illustrates a timing diagram of transponder in response to 15 the pulsed exciter signal in FIG. 9 with the time delay of the present invention.

FIG. 10 is a block diagram of electrostatic EAS reader in accordance to the present invention.

FIG. 11 is a block diagram of electrostatic EAS transponder in accordance to the present invention.

20 FIG. 12 is an exemplary schematic of electrostatic EAS transponder illustrated in FIG. 11.

#### Detailed Description of the Preferred Embodiments

In the following detailed description of the present invention,

25 numerous specific details are set forth in order to provide a thorough understanding of the present invention. Well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention. While the following detailed description of the present invention mainly describes its 30 application to electrostatic radio frequency identification (RFID) systems, it is to be appreciated that the present invention is equally applicable to other RFID systems such as electromagnetic, etc. Moreover, while the following detailed description of the present invention mainly describes its application to passive transponders (i.e., without its own power source), it

is to be appreciated that the present invention is also applicable to active transponders (i.e., with its own power source). Furthermore, while the following detailed description of the present invention is related to monopole systems, it is to be appreciated that the present invention is also 5 applicable to dipole systems.

The present invention provides an apparatus and system to combine a radio frequency identification (RFID) function with an electronic article surveillance (EAS) function in the same system that is inexpensive, easy to manufacture, and allows for packaging flexibility.

10 In a first embodiment, the present invention meets the above need with an electrostatic transponder comprising a plurality of electrodes, an analog interface module, a memory, a power on reset (POR) circuit, a modulator, and a controller. The analog interface module is coupled to the plurality of electrostatic electrodes. The analog interface module is used to 15 extract a power signal and a clock signal having a first carrier frequency from an exciter signal received by the plurality of electrostatic electrodes. The analog interface module then rectifies and regulates the exciter signal for use in activating the electrostatic RFID transponder. The POR circuit is connected to the analog interface module for preventing false data 20 transmission. As an example of a time delay, the POR circuit monitors a count of clock cycles in response to an enable signal being asserted.

The modulator is coupled to the memory. The modulator modulates data information stored in the memory with a second carrier frequency. The controller is coupled to the analog interface module and the memory. 25 The controller determines whether a RFID operating mode or an EAS operating mode is involved. If the RFID operating mode is involved, the controller asserts the enable signal. The controller reads data information from the memory and sends the data information to the analog interface module for transmitting over the plurality of electrostatic electrodes only if 30 the exciter signal is still being received when the time delay reaches a predetermined value. Conversely, if the EAS operating mode is involved, the controller disables the time delay and sends a alarm signal to the analog interface module for sending over the plurality of electrostatic electrodes.

In a second embodiment, the present invention meets the above need with an electrostatic transponder that comprises a first and second electrodes, a rectifier circuit, and a regulator circuit. The first and second electrodes are used for receiving an electrostatic exciter signal having a 5 first carrier frequency and for transmitting an electrostatic alarm signal having a second carrier frequency. The rectifier circuit is coupled to the first and second electrodes. The rectifier circuit rectifies the electrostatic exciter signal received to generate a voltage signal. The regulator circuit is coupled to the rectifier circuit. The regulator circuit maintains the voltage 10 signal in a desired voltage range. The regulator circuit provides a HIGH and a LOW voltage output to power the electrostatic EAS transponder. The clock extraction circuit is coupled to the first and second electrodes, the clock extraction circuit retrieves clock information from the exciter signal and generates a derivative clock signal having the second carrier 15 frequency based on clock information retrieved from the exciter signal.

The electrostatic EAS transponder may further include a load modulation circuit that is coupled to the clock extraction circuit and the first and second electrodes. The load modulation circuit generates the electrostatic alarm signal by varying an impedance across the first and 20 second electrodes.

All the features and advantages of the present invention will become apparent from the following detailed description of its preferred embodiment whose description should be taken in conjunction with the accompanying drawings.

25 The RFID technology implemented under the present invention is capacitance-based. In capacitance-based RFID technology, an electrostatic field is generated for use in activating the electrostatic RFID transponder (also known as tag) and transmitting information between the electrostatic RFID reader and electrostatic RFID transponder. In short, an 30 electrostatic field is an energy (electrical) field created between two electrodes having a voltage differential. Because electrodes (i.e., plates) are used (instead of coils) to transmit and receive electrostatic signals, integration of capacitance-based RFID technology with an integrated circuit is more manufacturable. The electrodes and associated electrical circuits

of electrostatic RFID systems can easily be implemented on flat and printable surfaces including paper, plastic, or synthetic substrates. Moreover, the manufacturing process involved is inexpensive and requires minimal components. As such, electrostatic RFID technology may be ideal for disposable applications.

5 In an embodiment of the present invention, an electrostatic RFID/EAS transponder acts both as a RFID transponder and as an EAS transponder. When the electrostatic RFID/EAS system is in RFID operating mode (i.e., transferring data between a transponder and a 10 reader), a delay period is introduced into the activation period of the electrostatic RFID/EAS transponder. The delay is used to ensure that the pulsed exciter signal generated by an electrostatic EAS reader does not falsely activate the electrostatic RFID/EAS transponder. In other words, the electrostatic RFID/EAS transponder can become activated for data 15 transfer only if the exciter signal is continuous for a time duration that is greater than the delay time. Conversely, when the electrostatic RFID/EAS transponder is in EAS operating mode, the time delay is disabled. The electrostatic RFID/EAS transponder then generates a theft prevention alarm signal to the electrostatic RFID/EAS reader.

20 FIG. 1 illustrates, for example, a system level diagram of an electrostatic RFID/EAS system in accordance with the first embodiment of the present invention. Electrostatic RFID/EAS system 100 has a RFID operating mode, which allows for contactless, bi-directional signal transfer between a reader and transponder, and an EAS operating mode for theft 25 prevention. In one of its many RFID applications, electrostatic RFID system 100 is a parcel/letter tracking system in which packages or letters placed on a conveyor belt are automatically tracked to determine identification information including sender's name and address, receiver's name and address, date ship, check-in station, time stamp, etc. It is to be 30 appreciated that electrostatic RFID system 100 is exemplary only and that the present invention can be implemented in a number of different electrostatic RFID systems including an inventory management system, an identification access system, an admission ticketing system, etc.

As shown in FIG. 1, electrostatic RFID system 100 includes electrostatic RFID/EAS reader 101, electrostatic RFID/EAS transponder 102, host computer system 103, and conveyor belt 104. Electrostatic RFID/EAS transponder 102 is one of a plurality of electrostatic RFID/EAS transponders that have been implemented as part of a shipping label that has been attached to a letter or package. Electrostatic RFID/EAS reader 101 can provide bi-directional data transfer to/from electrostatic RFID/EAS transponder 102 and vice versa. Conveyor belt 104 is set up so that the letters and packages when placed on the belt are within transmission range of electrostatic RFID/EAS reader 101 and electrostatic RFID/EAS transponder 102. The letters and packages placed on conveyor belt 104 are moving at a speed that allows sufficient time for the information to be transferred between reader 101 and transponder 102.

In general, electrostatic RFID/EAS reader 101 generates an electrostatic (electrical) field for use both as a power source for electrostatic RFID/EAS transponder 102 and for transferring information between electrostatic RFID/EAS reader 101 and electrostatic RFID/EAS transponder 102. As such, electrostatic RFID/EAS reader 101 electrostatically transmits a power/exciter signal to the surrounding space from the reader electrodes. The electrostatic power/exciter signal activates electrostatic RFID/EAS transponder 102 when the package to which it is attached comes within the transmitting range of reader 101. Upon being sufficiently energized, electrostatic RFID/EAS transponder 102 responds by electrostatically transmitting a read data signal carrying the information stored in its memory to electrostatic RFID/EAS reader 101 (as part of a read operation). It is to be appreciated that the power signal transmitted by electrostatic RFID/EAS reader 101 powers electrostatic RFID/EAS transponder 102 during its read and/or write operations.

The electrostatic read data signal received by electrostatic RFID/EAS reader 101 is demodulated, amplified, and filtered. The data carried by the read data signal is retrieved, decoded, and formatted as required prior to being transferred to host computer system 103. Upon receiving the formatted data, host computer system 103 may use the data to update its database. In the current example, host computer system 103

may update the information in its database to reflect the latest status of a package. Host computer system 103 may further processes the information received as required in a different application. For example, in an access ID application, host computer system 103 may compare the 5 information received with those already stored in its database to determine whether access should be granted or denied to the individual carrying the transponder.

Referring now to FIG. 2 illustrating in greater detail the components of electrostatic RFID/EAS reader 101. As shown in FIG. 2, electrostatic 10 RFID/EAS reader 101 comprises exciter 201, receiver 202, demodulator 203, processor 204, exciter electrode 205, and reader electrode 206. Exciter electrode 205 is coupled to exciter 201. Likewise, reader electrode 206 is coupled to receiver 202. Operationally, exciter 201 first generates 15 an exciter signal for activating transponder 102. Basically, the exciter signal provides operating power to electrostatic RFID/EAS transponder 102 in the form of electrostatic (electric) energy. In addition, the carrier frequency of the exciter signal provides clock information for transponder 102. In the preferred embodiment, the electrostatic exciter signal has a carrier frequency of 125 kHz. The electrostatic exciter signal is transmitted 20 to transponder 102 through exciter electrode 205. Additionally, exciter 201 may further generate and transmit a signal that carries a read mode data sequence. In response, RFID/EAS transponder 102 sends back the data stored in its memory if RFID/EAS transponder 102 is in RFID operating mode or an alarm signal if RFID/EAS transponder 102 is in EAS operating 25 mode. Such an alarm signal indicates that an article may be stolen or removed without authorization. Optionally, the alarm signal may include data, for example, if identification of the stolen or removed article is desired.

If a RFID operating mode is involved, upon receiving an electrostatic 30 read data signal from electrostatic RFID/EAS transponder 102 via reader electrode 206, receiver 202 first amplifies the read data signal. Receiver 202 also filters out unwanted frequency bands. Receiver 202 then provides the electrostatic read data signal to demodulator 203 which demodulates the read data signal according to a predetermined

demodulation scheme to retrieve the read data. In the preferred embodiment, depending on the modulation setting of transponder 102, the read data signal is modulated by a phase shift keying (PSK) modulation scheme. It is to be appreciated that other modulation schemes such as

5 amplitude shift keying (ASK), frequency shift keying (FSK) modulation, and others can also be used to modulate the read data signal. The electrostatic read data signal is then sent to processor 204 that decodes and formats the data as required by host computer 103. The formatted read data is then sent to host computer 103 for processing.

10 If an EAS operating mode is involved, upon receiving an electrostatic alarm signal, receiver 202 amplifies the alarm signal. Receiver 202 then sends the alarm signal to processor 204 which generates a signal to drive the desired type of alarm (e.g., audio, visual, etc). In general, no demodulation is required in EAS operating mode.

15 However, demodulation may be employed if it is desired that data be associated with the transponder.

Reference is now made to FIG. 3 illustrating in greater detail the components of electrostatic RFID/EAS transponder 102. As shown in FIG. 3, transponder 102 comprises analog interface module 301, power on reset (POR) circuit 302, bitrate generator 303, write decoder 304, charge pump 305, input register 306, controller 307, mode register 308, modulator 309, memory 310, pads/terminals 312-313, and electrostatic transponder electrodes 314 and 316. Electrostatic transponder electrodes 314 and 316 are coupled to power pads 312 and 313. Accordingly, pads 312-313 are used to couple transponder 102 to an operating power source via transponder electrodes 314 and 316. Moreover, since the exciter signal from reader 101 has a carrier signal that can be used as a clock signal, pads 312-313 provides the coupling to allow clock information to be sent to transponder 102 for synchronization purposes instead of requiring a clock oscillator. As such, pads 312-313 are sometimes known as clock pads. Furthermore, pads 312-313 provide the coupling to transponder electrodes 314 and 316 to allow read data to be transmitted from transponder 102 to reader 101. For optimum electrostatic performance, the total input capacitance between pads 312-313 must be minimized. In the preferred

embodiment, input capacitance is 5 pF or less. Circuitry may be employed in pads 312-313 to protect against electrostatic discharge (ESD). Pads 312-313 are preferably located at each far end of the silicon in order for optimal assembly methods to be employed. Analog interface module 301

5 is coupled to pads 312-313 and used to extract the exciter/power signal, clock signal, and data sequence signal from a signal received by electrostatic transponder electrodes 314 and 316.

FIG. 4 is a block diagram of analog interface module 301. As shown in FIG. 4, analog interface module 301 consists of full-wave rectifier circuit 401, regulator circuit 402, clock extraction circuit 403, gap detector circuit 405, and ESD protection circuit 406. ESD protection circuit 406 is designed to provide protection for transponder 102. Accordingly, any signals on pads 312-313 are governed by ESD protection circuit 406. Signals received from pads 312-313 are passed from ESD protection circuit 406 to full-wave rectifier circuit 401 which converts the input alternating-current (AC) voltage supplied by pads 312-313 into a direct-current (DC) voltage. The DC voltage is provided to regulator circuit 402 that ensures that the voltage level of the DC voltage signal stays within a desired range. The regulated voltages Vdd and Vss are used to power electrostatic transponder 102. Clock extraction circuit 403 extracts a clock signal from the exciter signal. This extracted clock signal is provided throughout transponder 102. In the preferred embodiment, clock extraction circuit 403 has a clock divider circuit to generate a second clock signal that has a carrier frequency that is different from the exciter carrier frequency

20 (i.e., 62.5 kHz). This second clock signal is eventually provided to modulator 309 (via controller 307) to use as a carrier signal in sending data from transponder 102 to RFID/EAS reader 101 in RFID operating mode. The second clock signal is also used as a carrier signal in sending an alarm signal to RFID/EAS reader 101 in EAS operating mode. Controller

25 307 generates such alarm signal.

In an alternate embodiment, clock extraction circuit 403 includes a second clock divider circuit to generate a third clock signal using the clock signal received from exciter 201. The third clock signal has a carrier frequency that is different from the both the first and second clock signals

(e.g., 31.25 kHz). This third clock signal is used as a carrier signal in transmitting an alarm signal from electrostatic RFID/EAS transponder 102 to electrostatic RFID/EAS reader 101 in EAS operating mode.

Gap detector circuit 405 is used to detect whether there is a start or field gap in the write data sequence received from reader/encoder 101 to transponder 102 during a RFID write mode. Such gaps indicate that a write mode is likely involved. If a start gap is detected, gap detector circuit 405 passes the write data sequence to write decoder 304. Otherwise, gap detector circuit 405 notifies controller 307 that a RFID read mode is involved. Modulator circuit 309 is used to provide load modulation dampening for sending read data signals from transponder 102 to reader/encoder 101 during RFID read mode.

Referring now back to FIG. 3, controller 307 controls access to memory 310. More particularly, under the right conditions, controller 307 writes data information received from electrostatic RFID reader 101 into memory 310 in response to a write command or retrieves (reads) data information from memory 310 and sends it to analog interface module 301 for transmission via the plurality of electrostatic transponder electrodes in response to a read command.

Modulator 309 modulates read data retrieved from memory 310 by controller 307 according to a selected modulation scheme during a read mode. In the preferred embodiment, the modulation scheme is PSK. Modulator 309 then sends the modulated read data signal to analog interface module 301 to relay to pads 312-313 which ultimately couples the read data signal through load modulation to reader 101 via transponder electrodes 103.

POR circuit 302 monitors the electrostatic exciter signal that has been rectified and regulated to determine whether a sufficient voltage has been generated to power on electrostatic RFID transponder 102. When sufficient voltage has been reached, POR 302 allows transponder activities to begin. In other words, following a reception of an exciter signal, POR circuit 302 determines whether a predetermined voltage threshold is reached by the DC voltage signal provided by regulator circuit 402 to power-up electrostatic RFID transponder 102. When this threshold is

reached, POR circuit 302 asserts an enable signal to so indicate. Otherwise, the enable signal is deasserted. This enable signal is provided to all major functional circuits of transponder 102 such as controller 307 to enable or disable the circuits.

- 5 Bitrate generator 303 receives as input the clock signal having a carrier frequency of 125 kHz from clock extraction circuit 403. Bitrate generator 303 generates the data transfer rate at which data is transferred from/to memory 310 during read and write mode, respectively. Bitrate generator 303 generates the data transfer rate by dividing the power
- 10 carrier frequency of 125 kHz by a predetermined factor. The data transfer rate is provided to controller 307. In the preferred embodiment, bitrate generator 303 can be programmed by the end user to operate at either 125 kHz/16 (7.81 kHz) or 125 kHz/32 (3.91 kHz).

When gap detector 405 detects that a write operation may be involved, it forwards the data sequence signal to write decoder 304. Write decoder 304 then decodes the data sequence signal to retrieve instruction, data, and address information related to the write operation. If it recognizes the codes as a write command, write decoder 304 signals to so notify controller 307. Write decoder 304 also verifies the validity of the data stream. The decoded instructions and information about the validity of the data stream are provided to controller 307.

In the preferred embodiment, memory 310 is an electrically erasable programmable read only memory (EEPROM) which has a capacity of 1,056 bits. Memory 310 is used to store write data received from reader 101 during write mode. The data is retrieved from memory 310 and electrostatically coupled to reader 101 during read mode. In general, high voltage is required to write data into an EEPROM. Hence, in write mode, charge pump 305 generates the required voltage to write data to memory 310. Because such voltage generally takes time to build up, the write data is first buffered in input register 306. In so doing, controller 307 is free to perform other tasks in the interim period. When the required write voltage is reached, the write data buffered in input register 306 is written into memory 310. In general, controller 307 controls all read and write memory access transactions. In addition, controller 307 loads configuration

information from the designated configuration (mode) memory block (block 0 of memory 310) into mode register 308. Such configuration block data is programmed in block 0 of memory 310 during the write mode and includes the operation (OP) codes as well as other configuration information that

5 controller 307 and modulator 309 are required to follow during a read operation. Accordingly, controller 307 and modulator 309 access the op-codes and configuration information stored in mode register 308 whenever necessary.

In the preferred embodiment, during RFID operating mode,

10 modulator 309 carries out the selected modulation scheme on all read data retrieved from memory 310 using the clock frequency of a signal derived from clock extraction circuit 403 and controller 307. It should be clear to a person of ordinary skill in the art that this signal can be generated by other means such as an internal oscillator. The modulated read data signal is

15 then sent to analog interface module 301. In the preferred embodiment, data is PSK encoded and coupled to reader 101 via load modulation. The modulation scheme can also be skipped all together such as when it is desirable to de-activate an EAS transponder. The modulation configuration information is stored in mode register 308 that is accessible

20 to modulator 309. During EAS operating mode, the time delay is disabled by controller 307. Alternatively, during EAS operating mode, controller 307 prevents data stored in memory 310 from being read and sent to analog interface module 301 for sending over electrostatic transponder electrodes 314 and 316.

25 Reference is now made to FIG. 5 illustrating an exemplary mapping of memory 310, which as discussed earlier, has a capacity of 1,056 bits. As illustrated in FIG. 5, memory 310 is organized into N individually addressable memory blocks each having a lock bit and 32 data bits. The first memory block (block 0) is designated as the configuration/mode block

30 for storing configuration (mode) information which includes a lock bit and configuration bits. The remaining memory blocks are designated for storing user data that includes a lock bit, synchronization bits, and user data bits. FIG. 6 illustrates the lock bit and some exemplary individual configuration bits in the configuration block (block 0). As shown in FIG. 6,

the configuration (mode) information includes locking information, POR delay information, data rate information, modulation type information, modulation enable information, max block information, and modulation threshold information, etc. The lock bit of the configuration block and user

5 blocks indicates whether the contents of the associated block can be altered. When the lock bit is asserted, the lock bit and the remaining contents of the associated block can not be altered. Otherwise, the lock bit and the remaining contents of the associated block can be rewritten (programmed).

10 The POR delay bit indicates whether a delay following the DC voltage signal generated by regulator circuit 402 reaching a predetermined voltage threshold is desired upon powering up. The added delay is used to overcome any false activation caused by EAS system. In other words, the added delay is introduced when electrostatic RFID/EAS transponder 102 is

15 operating in a RFID operating mode. Accordingly, when the POR delay bit is asserted (enabled) by the user, a delay is carried out by electrostatic RFID/EAS transponder 102 prior to transmitting read data from memory 310 to electrostatic RFID/EAS reader 101 at a second frequency. In the preferred embodiment, such frequency is 62.5 kHz. Otherwise, when the

20 POR delay bit is not asserted, electrostatic RFID/EAS transponder 102 is operating in an EAS operating mode. In that case, no such POR delay is implemented when the power voltage reaches the predetermined threshold voltage. In an alternate embodiment, controller 307 does not allow data to be transferred from memory 310 to electrostatic RFID/EAS reader 101

25 when the power voltage reaches the predetermined threshold voltage. Rather, electrostatic RFID/EAS transponder 102 sends back an alarm signal at a third carrier frequency. In one embodiment, the third frequency is equal to the second frequency of 62.5 kHz. In another embodiment, the third frequency is different from the second frequency.

30 The data rate information determines whether bitrate generator 303 is to operate at a data rate of either 7.81 kHz or 3.91 kHz. The modulation information determines the type of modulation. The modulation enable information enables/disables modulation. The modulation threshold information determines the magnitude of modulation to be carried out. The

max block information ('MAXBLK') determines the number of user data blocks (i.e., from block 1-to-block MAXBLK) to be cyclically transmitted to reader/encoder 101 in a read operation. MAXBLK can be any value between 0 and N. In read mode, data from memory 310 is serially

5 transmitted beginning with bit 1 of block 1 and ending with bit 32 of block MAXBLK. The data transmission of block 1 to block MAXBLK then repeats continuously in a cyclical fashion. For example, if MAXBLK is set to six (6), blocks 1-6 are cyclically and continuously transmitted. The contents of configuration block 0 is normally not transmitted. However, if MAXBLK is

10 set to zero (0), the contents of configuration block 0 can be read. Under the present invention, the information in configuration block 0 as well as all user data blocks 1-N are programmable by reader/encoder 101 or a substantially similar programming unit.

Reference is now made to FIG. 7 illustrating an exemplary POR circuit 302. As shown in FIG. 7, POR circuit 302 comprises counter circuit 701, comparator 702, AND-gate 703, and voltage source 704. Voltage from regulator circuit 402 is provided to the non-inverting input of comparator 702. The inverting input of comparator 702 is connected to the output of voltage source 704. The output of voltage source 704 is reference voltage  $V_{ref}$  that represents the predetermined voltage threshold. Essentially, this circuit is used to determine whether the DC (power) voltage from regulator circuit 402 has reached or exceeded the predetermined threshold. When the voltage from regulator circuit 402 has reached or exceeded such predetermined voltage threshold, comparator 25 702 outputs a HIGH voltage, which is used to enable controller 307. In so doing, activities, such as the loading of configuration/mode register 308, can begin. Moreover, even if the POR delay bit is not asserted indicating that the POR delay feature is not enabled, electrostatic RFID transponder 102 can start reading and transmitting data in memory 310 as soon as the 30 predetermined voltage threshold is exceeded. In accordance to the present invention, the output from comparator 702 is also provided as an input to AND-gate 703 which receives as its second input the output of counter circuit 701.

As discussed earlier, the configuration/mode information from block 0 of memory 310 is loaded into mode register 308 upon activation. By reading the configuration information in mode register 308, controller 307 determines whether the POR delay feature is enabled. If the POR delay 5 bit is asserted indicating that the POR delay feature is enabled and that RFID/EAS transponder 102 is in a RFID operating mode, controller 307 sends an enable signal to counter circuit 701 and waits for a return signal from AND-gate 703 before reading and transmitting data from read memory 310 at the second frequency 62.5 kHz. On the other hand, if the 10 POR delay bit is deasserted indicating that the POR delay feature is disabled and that RFID/EAS transponder 102 is in an EAS operating mode, controller 307 disables counter circuit 701 and sends modulated data at the third or second carrier frequency as soon as the output signal of comparator 702 signals that the predetermined voltage threshold is 15 exceeded. Alternatively, in the EAS operating mode, controller 307 prevents data from being read from memory 310 and sends an alarm signal at the third carrier frequency when the output signal from comparator 702 indicates that the predetermined voltage threshold is exceeded.

Counter circuit 701 receives as input the clock signal, which has 20 been retrieved by clock extraction circuit 403. When enabled, counter circuit 701 resets and starts counting the clock cycles in the clock signal received, which as discussed earlier, has a frequency of 125 kHz. In the preferred embodiment, when the clock count in counter circuit 701 reaches the predetermined value which is equal to a predetermined delay based 25 upon the clock signal frequency, counter circuit 701 generates a HIGH output signal. Before the clock count reaches the predetermined value or when counter circuit 701 is not enabled, counter circuit 701 outputs a LOW signal. The output signal from counter circuit 701 is provided as a second input to AND-gate 703. Accordingly, for AND-gate 703 to output a HIGH 30 output signal, a delay T1 following the first reception of exciter signal has occurred and the DC (power) voltage from regulator circuit 402 needs to reach the predetermined threshold. AND-gate 703 provides its output to controller 307 to indicate whether data from memory 310 should be transmitted to electrostatic reader 101.

FIGS. 8, 8A, 8B, 9, 9A, and 9B are timing diagrams that illustrate the operation concept of POR circuit 302. More particularly, FIG. 8 illustrates a continuous exciter signal generated by electrostatic RFID/EAS reader 101 during RFID operating mode.

5 FIG. 8A illustrates a timing diagram of transponder 102 in response to the continuous exciter signal in FIG. 8 without the time delay of the present invention. As shown in FIG. 8A, transponder 102 starts communicating to reader 101 following a short start up time T0.

10 FIG. 8B illustrates a timing diagram of transponder 102 in response to the continuous exciter signal in FIG. 8 with the time delay of the present invention. As shown in FIG. 8B, transponder 102 only starts communicating to reader 101 following a time delay T1. The benefits associated with this delay is more clearly demonstrated when viewed together with a pulsed exciter signal generated by an EAS reader.

15 FIG. 9 illustrates a pulsed exciter signal generated by an EAS reader during EAS operating mode. For comparison purposes, the exciter signals in FIG. 8 and 9 are aligned in time. As shown in FIG. 9, the pulsed exciter signal from an EAS reader is alternately turned on for a time T2 and turned off for a time period T3.

20 FIG. 9A illustrates a timing diagram of transponder 102 in response to the pulsed exciter signal generated by an EAS reader shown in FIG. 9 without the time delay of the present invention. As shown in FIG. 9A, transponder 102 starts communicating to reader 101 following the short start up time T0. Communication continues for as long as the exciter signal remains on. Communication is halted when the exciter signal is turned off. For obvious reasons, such false activation is undesirable.

25 Conversely, FIG. 9B illustrates a timing diagram of transponder 102 in response to the pulsed exciter signal generated by the EAS reader with the time delay of the present invention. As shown in FIG. 9B, no data transfer is carried out by transponder 102 due to the time delay T1 of the present invention. This is so because the exciter signal must remain ON when the time delay T1 expires for transponder 102 to communicate with reader 101. Since T2 is less than T1, the exciter signal is turned off before

the time delay T1 expires. For this reason, false activation of transponder 102 is prevented.

The prior discussion describes the first embodiment of the present invention, an electrostatic RFID system that acts both as a RFID system and as an EAS system. The second embodiment of the present invention 5 involves an electrostatic EAS system having an electrostatic EAS reader 101' such as depicted in FIG. 10 and an electrostatic EAS transponder 102' such as depicted in FIG. 11 is now described.

Reference is now made to FIG. 10 illustrating electrostatic EAS 10 reader 101'. As shown in FIG. 10, electrostatic EAS reader 101' comprises exciter 1001, receiver 1002, alarm circuit 1003, exciter electrode 1005, and reader electrode 1006. Exciter electrode 1005 is coupled to exciter 1001. Reader electrode 1006 is coupled to receiver 1002. Operationally, exciter 1001 generates an exciter signal for activating electrostatic EAS 15 transponder 102'. Basically, the exciter signal provides operating power to electrostatic EAS transponder 102' in the form of electrostatic (electric) energy. In addition, the carrier frequency of the exciter signal provides clock information for electrostatic EAS transponder 102'. In the preferred embodiment, the electrostatic exciter signal has a carrier frequency of 125 20 kHz. The electrostatic exciter signal is transmitted to electrostatic EAS transponder 102' through exciter electrode 1005. In response, electrostatic EAS transponder 102' sends back an alarm signal to indicate that the article may be removed without authorization.

Upon receiving an electrostatic alarm signal from electrostatic EAS 25 transponder 102' via receiver electrode 1006, receiver 1002 first amplifies the alarm signal. Receiver 1002 also filters out unwanted frequencies. Receiver 1002 then sends the alarm signal to alarm circuit 1003. Alarm circuit 1003 generates the proper signal to drive the desired alarm type (e.g., audio, visual, etc.) to indicate that an article is being removed without 30 authorization. Alarm circuit 1003 has an alarm reset signal to deassert the drive signal when the alarm is to be deactivated.

Referring now to FIG. 11 illustrating an embodiment of electrostatic EAS transponder 102'. In general, EAS transponder 102' comprises rectifier circuit 1101, regulator circuit 1102, clock extraction circuit 1103,

load modulation (backscatter) circuit 1104, and transponder electrodes 1114 and 1116. Rectifier circuit 1101 converts the exciter signal received over transponder electrodes 1114 and 1116 into a full wave voltage signal. This full wave voltage signal is then provided as input to regulator circuit 1102 which ensures that the full wave voltage signal are maintained in a predetermined range. Regulator circuit 1102 supplies a regulated voltage signal to power the components of EAS transponder 102'. The exciter signal having a first carrier frequency (e.g., 125 kHz) from transponder electrodes 1114 and 1116 is also provided to clock extraction circuit 1103 that retrieves clock information from the exciter signal and generates a derivative clock signal having a second carrier frequency (e.g., 62.5 kHz) based on the clock information from the exciter signal. Clock extraction circuit 1103 provides the derivative clock signal to load modulation (backscatter) circuit 1104. Load modulation circuit 1104 varies the voltage differential across electrodes 1114 and 1116 by varying the impedance/resistance across electrodes 1114 and 1116. The varying voltage differential across electrodes 1114 and 1116 reflects an electrostatic field response signal having the second carrier frequency (e.g., 62.5 kHz) to electrostatic EAS reader 101'. Electrostatic EAS transponder 102' can be permanently deactivated by sending a exciter signal to EAS transponder 102' that has an energy level that is excessive compared to the energy level that EAS transponder 102' can tolerate without damage. Such an excessive energy level is designed to render EAS transponder 102' permanently inoperable.

In an alternate embodiment, load modulation circuit 1104 can be replaced by a third transponder electrode 1118 shown in dotted lines in FIG. 11. In this alternate embodiment, a signal having the second carrier frequency (e.g., 62.5 kHz) is transmitted to electrostatic EAS reader 101 over transponder electrode 1118.

FIG. 12 is an exemplary schematic of electrostatic EAS transponder 102' illustrated in FIG. 11. As shown in FIG. 12, rectifier circuit 1101 is made up of N-type field effect transistor (NFET) transistors 1210-1211 and diodes 1212-1213. Regulator circuit 1102 is made up of zener diode 1214 and capacitor 1215. Clock extraction circuit 1103 is made up of inverter

1216 and frequency conversion circuit 1217. Load modulation circuit 1104 is made up of resistor 1218 and NFET transistor 1219. In rectifier circuit 1101, the sources of NFET transistors 1210-1211 are connected together at node 1260. The gate of NFET transistor 1210 is connected to the drain 5 of NFET transistor 1211. The gate of NFET transistor 1211 is connected to the drain of NFET transistor 1210. The drain of NFET transistor 1210 is connected to transponder electrode 1116, and the drain of NFET transistor 1211 is connected to transponder electrode 1114. The drain of NFET transistor 1210 is also connected to the anode terminal of diode 1212. The 10 drain of NFET transistor 1211 is also connected to the anode terminal of diode 1213. The cathode terminals of diodes 1212 and 1213 are connected together at node 1270.

In the first half cycle of the exciter signal, when the voltage at transponder electrode 1114 is HIGH and the voltage at transponder 15 electrode 1116 is LOW, transistor 1210 is turned on and transistor 1211 is turned off. As a result, a HIGH voltage Vdd or a positive voltage is supplied to node 1270 and a LOW voltage Vss or a negative voltage is supplied to node 1260.

In the second half cycle, when the voltage at transponder electrode 20 1114 is LOW and the voltage at the transponder electrode 1116 is HIGH, transistor 1210 is turned off and transistor 1211 is turned on. As a result, a HIGH voltage Vdd or a positive voltage is still supplied to node 1270 and a LOW voltage Vss or a negative voltage is still supplied to node 1260. Hence, rectifier circuit 1101 is a full-wave rectifier.

25 In regulator circuit 1102, zener diode 1214 and capacitor 1215 are connected to nodes 1270 and 1260, and in parallel with each other. Zener diode 1214 has a cathode terminal and an anode terminal. The cathode terminal of zener diode 1214 is connected to node 1270 and the anode terminal of zener diode 1214 is connected to node 1260. Zener diode 1214 is used to shunt (clam) the differential voltage between nodes 1260 30 and 1270 to a predetermined maximum voltage. On the other hand, capacitor 1215 is used to smooth out the ripple of the differential voltage. In short, zener diode 1214 and capacitor 1215 are used to maintain the differential voltage within a predetermined range. In clock extraction circuit

1103, the input of inverter 1216 is connected to transponder electrode 1116. Inverter 1216 converts the sinusoidal waveform of the exciter signal into a square waveform. The square waveform output from inverter 1216 is provided as an input to frequency conversion circuit 1217. Frequency conversion circuit 1217 converts the carrier frequency of the square waveform into the second carrier frequency. Accordingly, frequency conversion circuit 1217 can be a clock divider circuit or a clock multiplication circuit. In the current embodiment, frequency conversion circuit 1217 is a divide-by-two circuit. It should be clear that other frequency conversion circuits can also be used. Frequency conversion circuit 1217 outputs a signal having the second carrier frequency to load modulation circuit 1104.

In load modulation circuit 1104, the gate of NFET transistor 1219 is connected to the output of frequency conversion circuit 1217, the source of NFET transistor 1219 is connected to node 1260, and the drain is connected to resistor 1218 which in turn is connected to electrostatic electrode 1116. As such, the output signal of frequency conversion circuit 1217 turns on and off transistor 1219 to dampen the differential voltage across electrostatic electrodes 1116 and 1114. When transistor 1219 is on, its source current returns to electrostatic electrode 1114 through transistors 1210 and 1211 in the full wave rectifier. In other words, the impedance across the two nodes is varied thereby introducing a voltage change in the differential voltage as desired.

Two embodiments of the present invention are thus described. In a first embodiment, both RFID function and EAS function are combined in the same electrostatic-based system. One advantage of such electrostatic RFID/EAS system is versatility. Other advantages of such electrostatic RFID/EAS system are its low costs, ease of manufacturability, and packaging flexibility. These advantages makes it practical to use such an electrostatic RFID/EAS system in high volume and low cost applications such as disposable applications.

In the second embodiment, an electrostatic EAS system is described. Advantages of such an electrostatic EAS system are its low

costs and ease of manufacturability. Another advantage of such electrostatic EAS system is that it allows for packaging flexibility.

While the present invention has been described in particular embodiments, the present invention should not be construed as limited by 5 such embodiments, but rather construed according to the claims below.

What is claimed is:

## CLAIMS

- 5 1. An electrostatic transponder comprising:
  - a plurality of electrodes;
  - an analog interface module coupled to the plurality of electrodes, the analog interface module extracting a power signal and a clock signal having a first carrier frequency from an exciter signal received by the
- 10 10 plurality of electrodes, the analog interface module rectifying and regulating the exciter signal for use in activating the electrostatic transponder;
  - a memory;
  - a power on reset (POR) circuit connected to the analog interface module for preventing false data transmission, the POR circuit
- 15 15 implementing a time delay in response to an enable signal being asserted;
  - a modulator coupled to the memory, the modulator modulating data information stored in the memory with a second carrier frequency; and
  - a controller coupled to the analog interface module and the memory, the controller determining whether a radio frequency identification (RFID)
- 20 20 operating mode or an electronic article surveillance (EAS) operating mode is involved, if the RFID operating mode is involved, the controller asserting the enable signal, the controller reading data information from the memory and sending the data information to the analog interface module for communication over the plurality of electrodes if the exciter signal is still
- 25 25 received when the time delay expires, if the EAS operating mode is involved, the controller sending an alarm signal to the analog interface module for communication over the plurality of electrodes.
2. The electrostatic transponder of claim 1, wherein the controller
- 30 30 disables the time delay if the EAS operating mode is involved.
3. The electrostatic transponder of claim 1, wherein the controller prevents data information stored in the memory from being sent to the

analog interface module for communication over the plurality of electrodes if the EAS operating mode is involved.

4. The electrostatic transponder of claim 3, wherein the alarm signal has one of the second carrier frequency and a third carrier frequency.
5. The electrostatic transponder of claim 1 further comprising a clock extraction circuit coupled to at least one of the plurality of electrodes, the clock extraction circuit retrieving clock information from the exciter signal and generating a derivative clock signal having the second carrier frequency based on clock information retrieved from the exciter signal.
- 10
6. The electrostatic transponder of claim 1 further comprising a load modulation circuit coupled to the modulator and at least one of the plurality of electrodes, the load modulation circuit communicating an electrostatic signal for communication by varying an impedance across the plurality of electrodes.
- 15
7. An electrostatic transponder comprising:
  - 20 a first electrode and a second electrode for receiving an electrostatic exciter signal having a first carrier frequency and for transmitting an electrostatic alarm signal having a second carrier frequency;
  - 25 a rectifier circuit coupled to the first electrode and the second electrode, the rectifier circuit rectifying the electrostatic exciter signal received to generate a voltage signal; and
  - 30 a regulator circuit coupled to the rectifier circuit, the regulator circuit maintaining the voltage signal in a desired voltage range, the regulator circuit providing a HIGH and a LOW voltage output to power the electrostatic EAS transponder.
- 30
8. The electrostatic transponder of claim 7, wherein the rectifier circuit comprises:
  - 20 a first NFET transistor having a source, a gate, and a drain, the drain of the first NFET transistor is connected to the first electrode;

a second NFET transistor having a source, a gate, and a drain, the source of the first NFET transistor is connected to the source of the second NFET transistor together at a first node, the gate of the first NFET transistor is connected to the drain of the second NFET transistor, the gate 5 of the second NFET transistor is connected to the drain of the first NFET transistor, and the drain of the second NFET transistor is connected to the second electrode;

10 a first diode having an anode terminal and a cathode terminal, the drain of the first NFET transistor is connected to the anode terminal of the first diode; and

15 a second diode having an anode terminal and a cathode terminal, the drain of the second NFET transistor is connected to the anode terminal of second diode, the cathode terminal of the first diode and the cathode terminal of the second diode are connected together at a second node which provides a positive voltage, the first node provides a negative voltage.

9. The electrostatic transponder of claim 7, wherein the regulator circuit comprises:

20 a zener diode having a cathode terminal and an anode terminal, the cathode terminal of the zener diode connected to the positive voltage, the anode terminal of the zener diode connected to the negative voltage; and a capacitor connected in parallel with the zener diode.

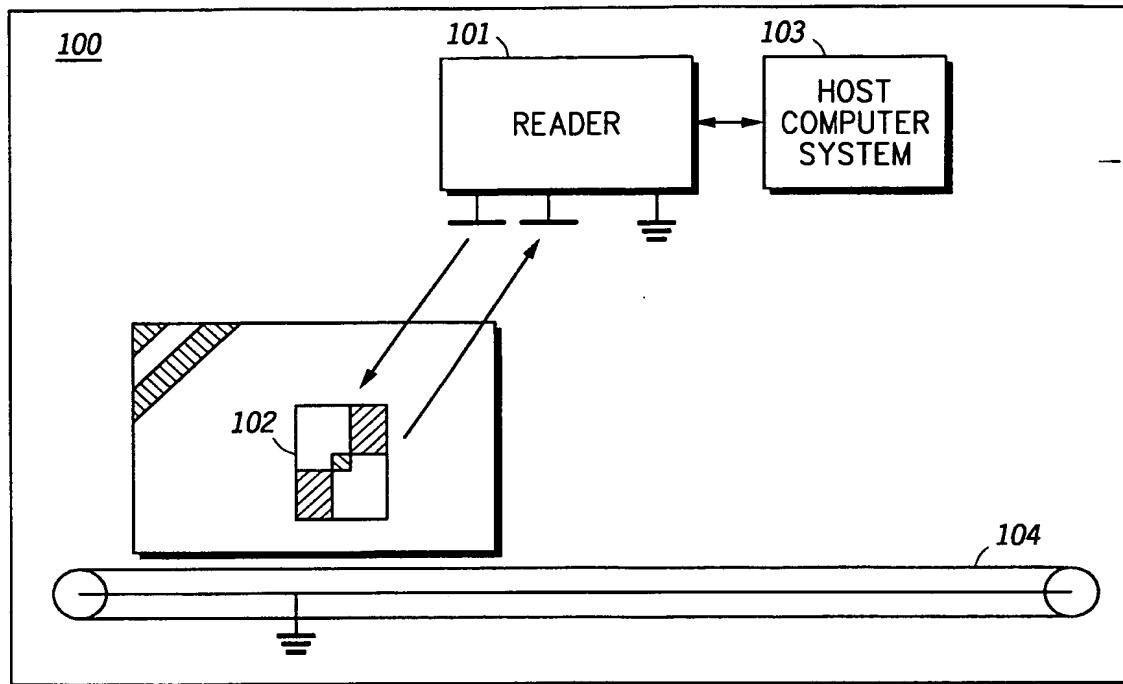
25 10. The electrostatic transponder of claim 7 further comprising a clock extraction circuit coupled to at least one of the first and second electrodes, the clock extraction circuit retrieving clock information from the electrostatic exciter signal and generating a derivative clock signal having the second carrier frequency based on clock information retrieved from the

30 electrostatic exciter signal.

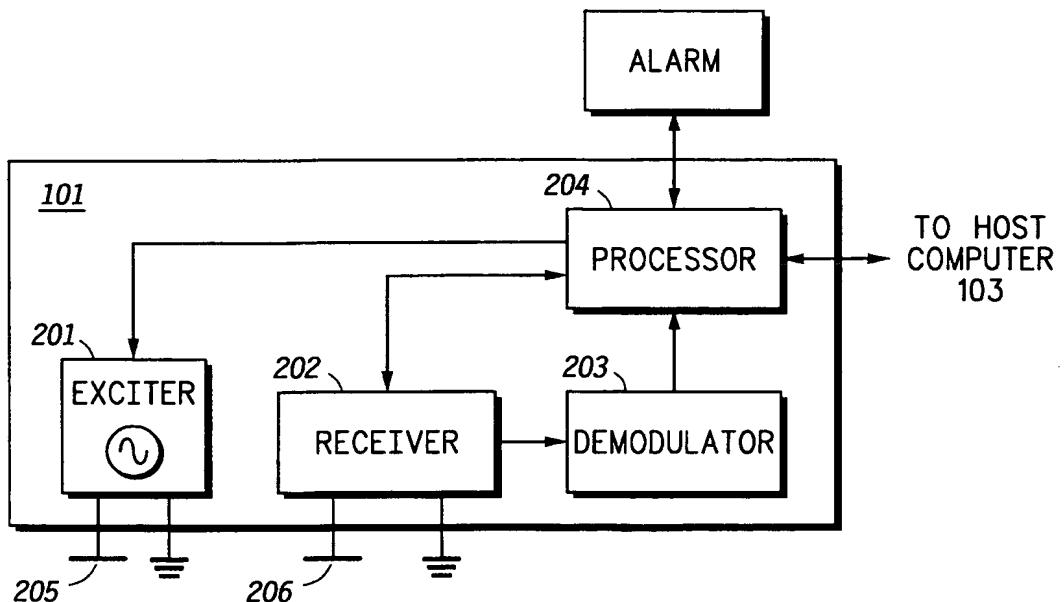
11. The electrostatic transponder of claim 10 further comprising a load modulation circuit coupled to the clock extraction circuit and at least one of the first and second electrodes, the load modulation circuit generating the

electrostatic alarm signal by varying an impedance across the first and second electrodes.

12. The electrostatic transponder of claim 11, wherein the load modulation circuit comprises:
  - 5 a resistor connected to the first electrode; and
  - a NFET transistor connected to the resistor and the LOW voltage output.
- 10 13. The electrostatic transponder of claim 10 further comprising a third electrode for transmitting the electrostatic alarm signal.
14. The electrostatic transponder of claim 10, wherein the clock extraction circuit comprises:
  - 15 an inverter connected to the first electrode or the second electrode; and
  - a frequency conversion circuit connected to the inverter, the frequency conversion circuit generating a derivative clock signal having the second carrier frequency based on clock information retrieved from the
  - 20 electrostatic exciter signal.
15. The electrostatic transponder of claim 14, wherein the frequency conversion circuit is a divide-by-two circuit.



*FIG. 1*



*FIG. 2*

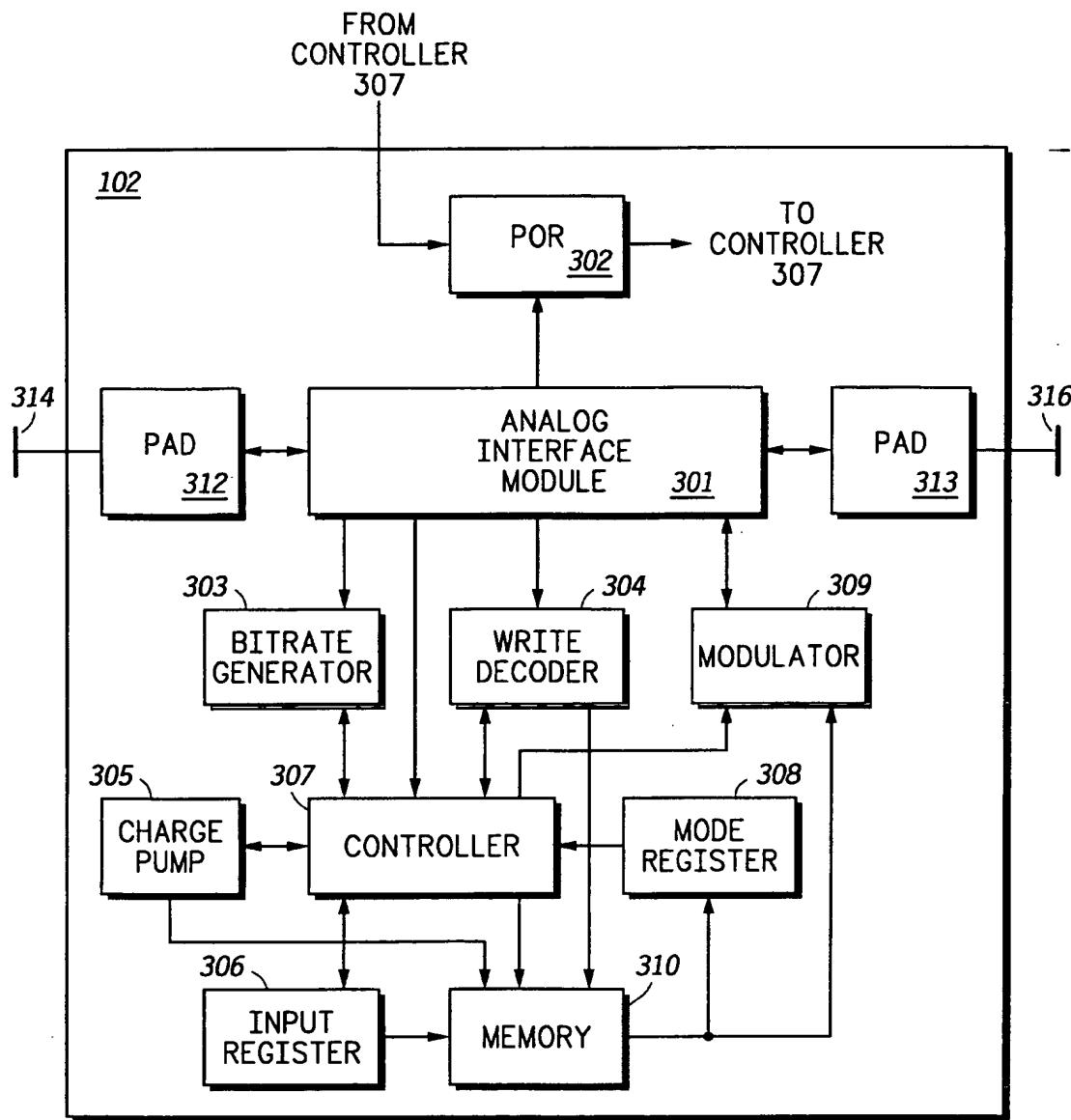
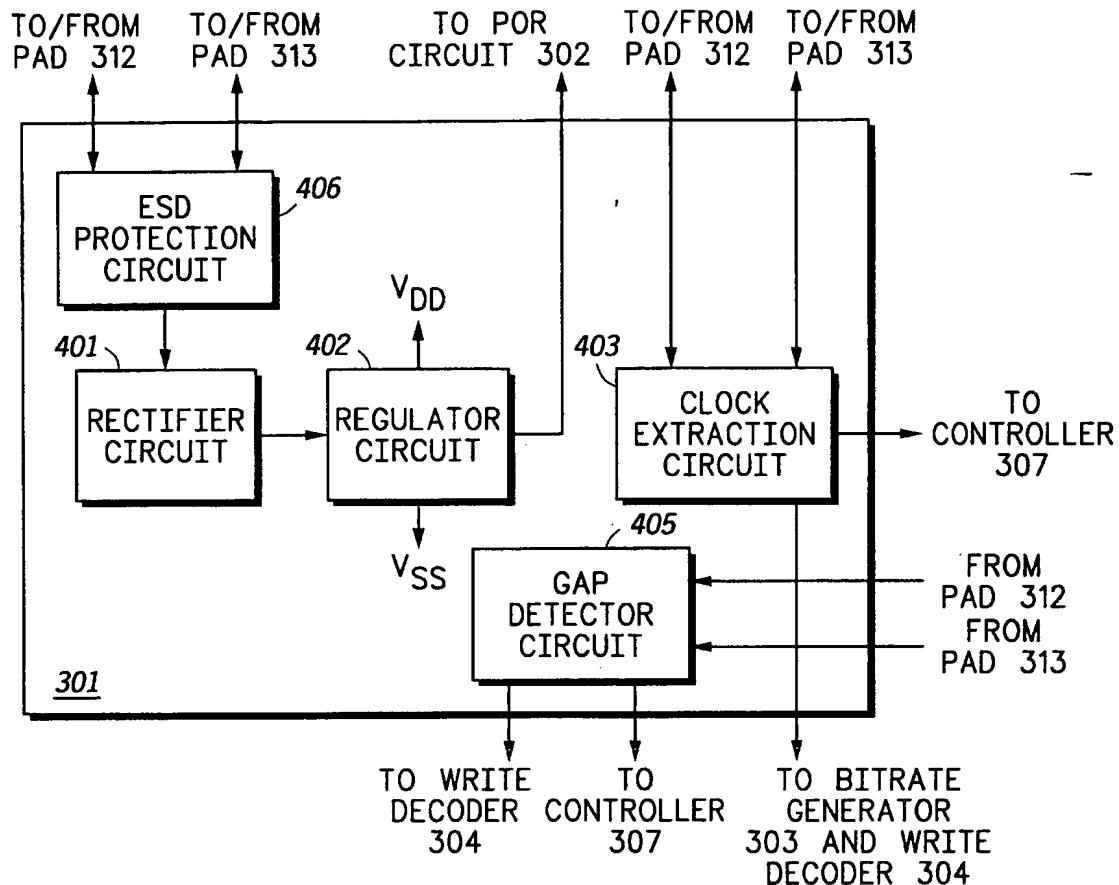


FIG. 3

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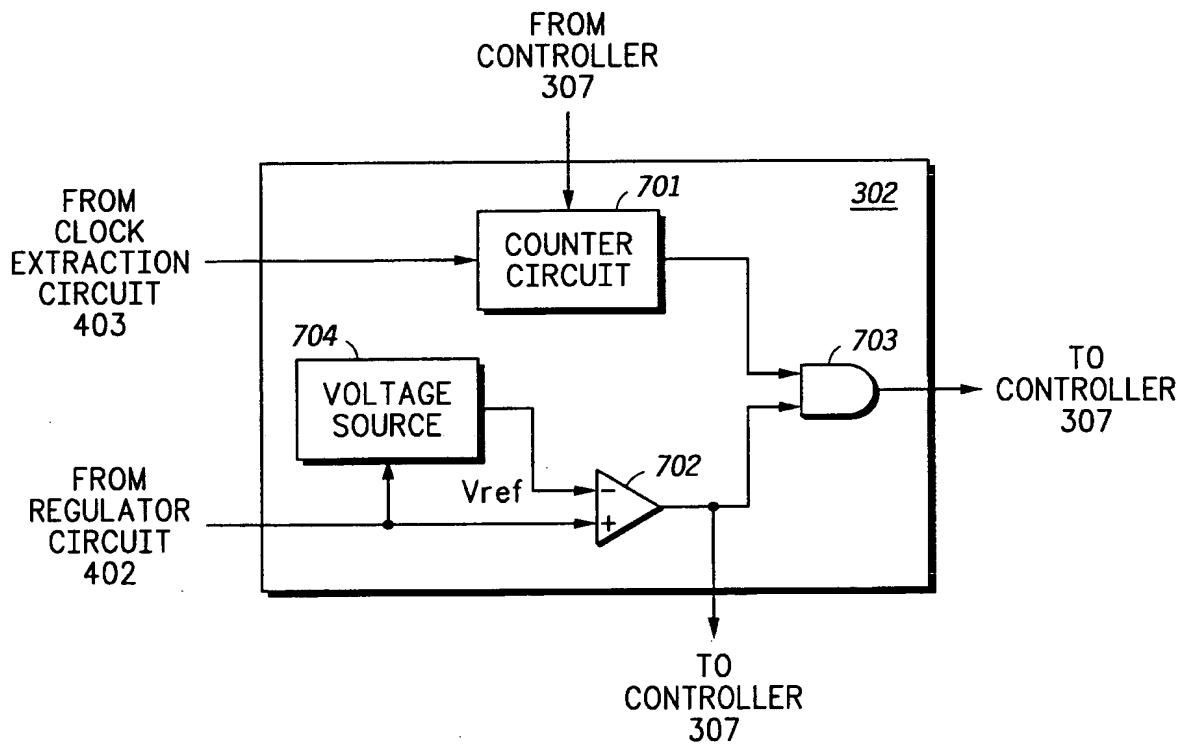
**FIG.4**

0	1	---	L
CONFIGURATION BITS			BLOCK 0
L	SYNC BITS	USER DATA BITS	BLOCK 1
L	SYNC BITS	USER DATA BITS	BLOCK 2
:			:
L	SYNC BITS	USER DATA BITS	BLOCK 29
L	SYNC BITS	USER DATA BITS	BLOCK 30
L	SYNC BITS	USER DATA BITS	BLOCK N

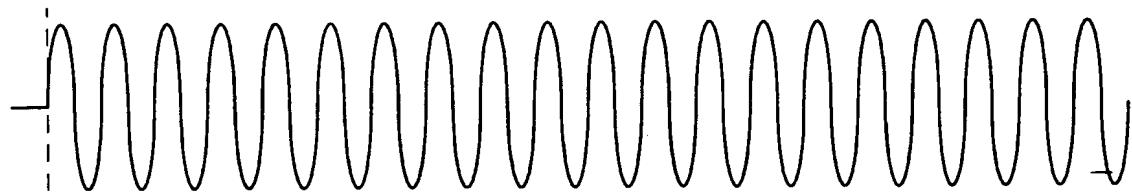
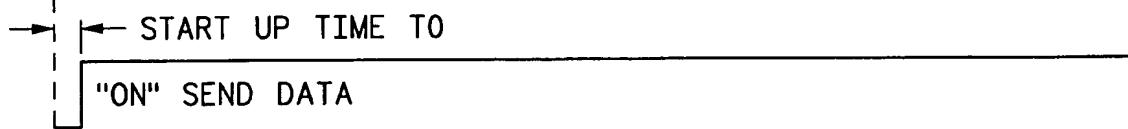
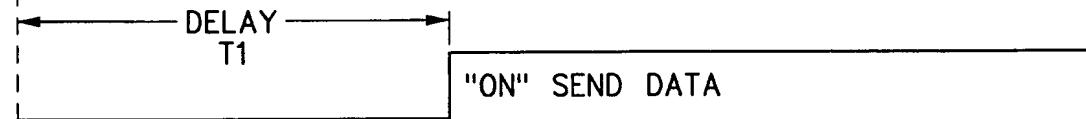
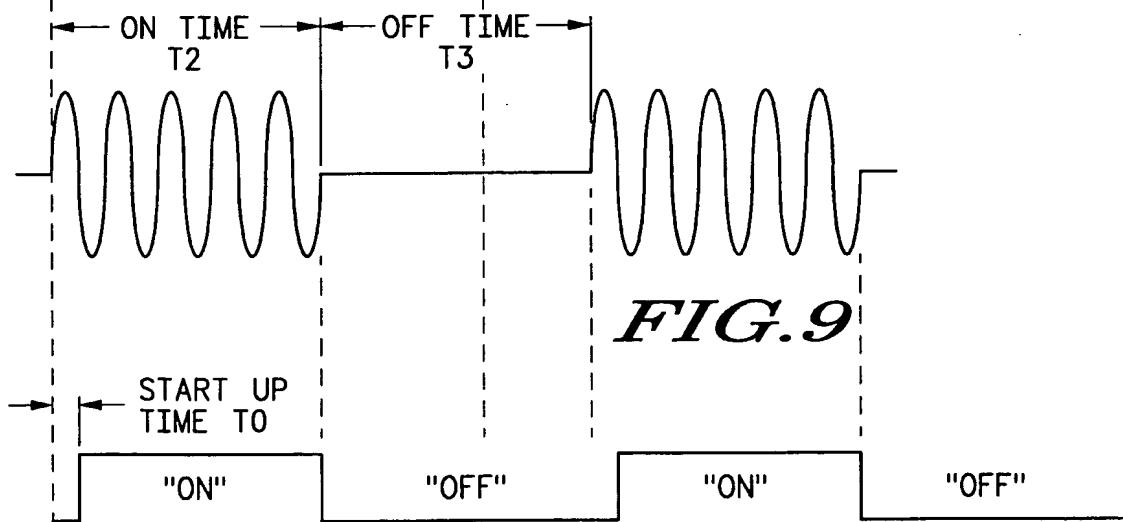
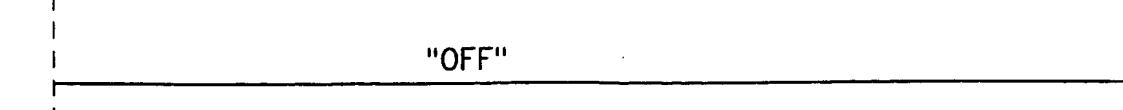
**FIG.5**

4/6

0	1	2	3	4	5	-----	L
LOCK BIT	POR DELAY	DATA RATE	MOD TYPE	MOD ENABLE	MOD LEVEL		MAX BLOCK ("MAXBLK")

*FIG. 6**FIG. 7*

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***FIG.8******FIG.8A******FIG.8B******FIG.9******FIG.9A******FIG.9B***

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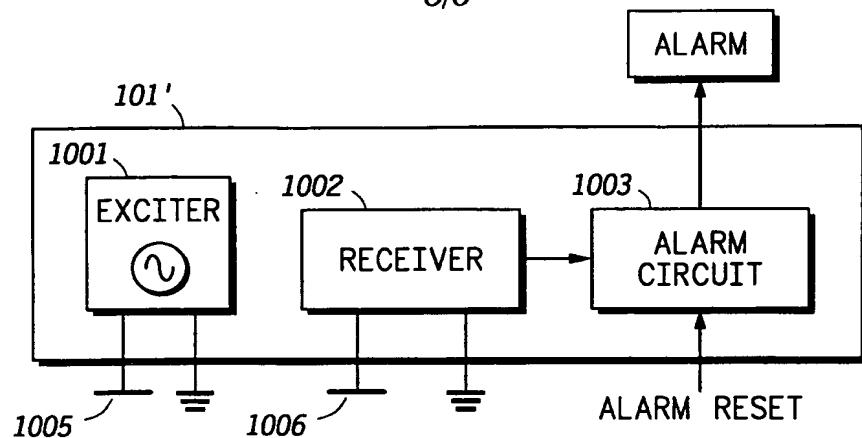


FIG.10

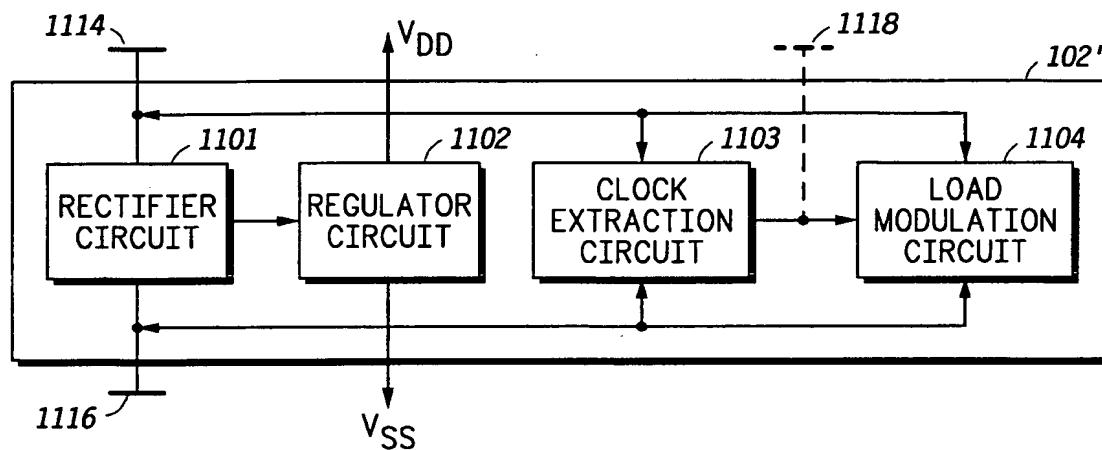


FIG.11

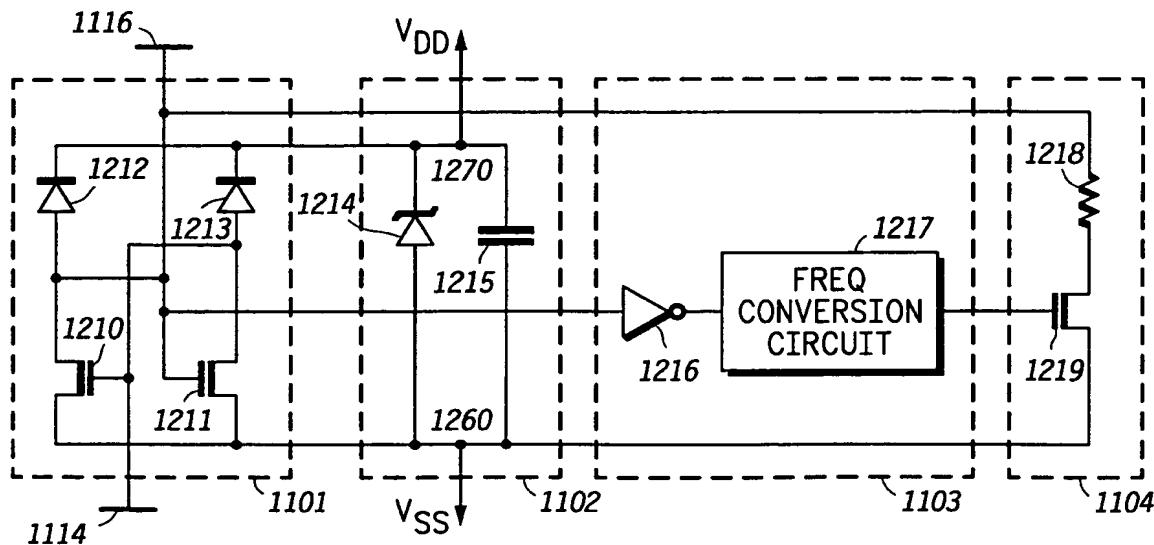


FIG.12

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/20803

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/825.54, 825.72, 870.31, 870.37; 152/152.1, 526, 539, 548; 342/44; 235/487

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,911,217 A (DUNN et al.) 27 March 1990, Figs. 6-10 and 15-24 and corresponding disclosure.	7 and 10-15
---		-----
A		1-6 and 8-9
A	US 4,742,470 A (JUENGEL) 03 May 1988, Fig. 12 and corresponding disclosure.	1-15
A	US 4,835,373 A (ADAMS et al.) 30 May 1989, Abstract and Figs. 1-2.	1-15
A	US 4,794,393 A (IMRAN) 27 December 1988, Abstract and Fig. 7.	1-15
Y	US 5,345,231 A (KOO et al.) 06 September 1994, Abstract and Figs. 1-2.	7 and 10-15
---		-----
A		1-6 and 8-9

 Further documents are listed in the continuation of Box C. 

See patent family annex.

•	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
•A•	document defining the general state of the art; is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
•B•	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
•L•	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
•O•	document referring to an oral disclosure, use, exhibition or other means		
•P•	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

06 DECEMBER 1999

Date of mailing of the international search report

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Joni Hill

INTERNATIONAL SEARCH REPORT

International application No.:  
PCT/US99/20803

A. CLASSIFICATION OF SUBJECT MATTER:  
IPC (6):

G08C 19/00, 19/06, 19/12; B60C 19/00, 9/00, 15/00, 9/02; G01S 13/74; G06K 19/00

A. CLASSIFICATION OF SUBJECT MATTER:  
US CL :

340/825.54, 825.72, 870.31, 870.37; 152/152.1, 526, 539, 548; 342/44; 235/487